The University of Jordan

King Abdullah II School for Information Technology			
Computer Science Department			
Year:	2016	**Semester:**	Fall

Course Information

Course Title & Number	Parallel Architecture (CS 1901754)
Prerequisite	------
Course Website	
Instructor	Prof. Mohammad Obaidat
Office Location	KASIT, CS Department
Office Phone	06-5355000 Ext. 22564
Office Hours	Sunday and Tuesday, 8:30am-10:00am Or by Appointment
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Course Description

Study of parallel processing hardware, memory, buses, multi-stage networks. Pipeline, array and associate processor, bus based systems, cross-bar systems, grids, systolic arrays, trees, and data-flow architecture. Processors for parallel architectures, memory structures, cache memory, bus structures. Arbitration and synchronization. Dynamically reconfigurable architecture.

References

References	1. Scalable Parallel Computing: Technology, Architecture and Programming by Kai Hwang and Zhiwei Xu, McGraw-Hill, 1998. 2.Advanced Computer Architecture: Parallelism, Scalability, Programmability, by Kai Hwang, McGraw-Hill Higher Education, First Edition, 1992. 3. Parallel Computer Architecture by David E. Culler and J. P. Singh, Morgan Kaufmann, 1999. 4. Advanced Computer Architecture: Parallelism, Scalability, and Programmability by Kai Hwang, McGraw-Hill, 1993. 5. Advanced Computer Architecture and Parallel Processing by Hesahm El-Rewini and Mostafa Abd-Elbarr, Wiley, 2004. 6. High Performance Computer Architecture by Harold S. Stone, Second edition, Addison-Wesley, 1990 7.Introduction to Parallel Algorithms and Architecture By F.T. Leighton, Morgan Kaufmann, 1992 9. Computer Architecture and Parallel Processing by Kai Hwang and Faye Briggs, McGrw-hill, 1984 8. Parallel Computing: Theory and comparison by G.J. lipovski and M. Miroslaw, Wiley intescience, 1987. 10. Shared Memory Multiprocessing, Edited by N. Suzuki, MIT Press, 1992. 11.Introduction to Parallel Computing, by Ananth Grama, Anshul Gupta, George Karypis, and Vipin Kumar, Addison-Wesley an imprint of Pearson Education, Second Edition, 2003. 12.Computer Organization & Design: The Hardware / Software Interface, by David A. Patterson and John L. Hennessy, Morgan Kaufmann Publishers, Inc., Third Edition, 2005. 13.Computer Architecture: A Quantitative Approach, by J. L. Hennessy & D. A. Patterson, Morgan Kaufmann Publishers, Inc., Forth Edition, 2006.

Assessment Policy		
Assessment Type	**Tentative Expected Due Date**	**Weight**
Research Term Paper	6th Week of Semester	20%
Midterm Exam/Programming Project	11th Week of Semester	30%
Final Exam	In Class as per University Exam Schedule	50%

Course Objectives

1. To acquaint with the essential aspects of parallel processing systems.
2. To introduce the parallel computing paradigms and scalability principle.
3. To explain conditions of parallelism, program partitioning and scheduling, and data and resource dependence.
4. To acquaint with the design and performance issues of parallel systems and their interconnection networks.
5. To develop good knowledge about multiprocessors, multicomputers, and massively parallel systems along with case studies.

Teaching & Learning Methods

- Class lectures, lecture notes, and research project are designed to achieve the course objectives.

- You are responsible for all material covered in the class.

- Please communicate with me regarding any concerns or issues related to Parallel Architecture by either in class or email.

- Lecture notes and syllabus will available on line.

Learning Outcomes

- ❖ Upon successful completion of this course, students:
  - Should be able to know basic terms associated with Parallel and Distributed Architecture, such as Message Passing, Multiprocessors, etc.
  - Should be able to know the structure of different Parallel and Distributed Architecture.
  - Should be able to know basic terms associated with Computer Architecture, such as MIPS, Throughput, Performance, Pipelining, etc.
  - Should be able to measure performance of different architectures.
  - Should be able to understand the design of the pipelined datapath and pipelined control of the MIPS architecture.
  - Should be able to design cache memory using direct mapping, set associative, and fully associative.

Course Content	
Sequence	**Topics**

(1)	Parallel computer platforms and models
	        -evolution of parallel computing/processing
	        -parallel processing applications
	        -PRAM models
	        -Scalability and its dimension
	        -architectural developments and tracks
	        -Clustering
	        -parallelism issues

(2)	Program development and network properties
	        -conditions of parallelism
	        -program partitioning and scheduling
	        -program flow mechanisms
	        -parallel system interconnects

(3)	Principle of scalable performance in parallel processing systems
	        -performance metrics and measures
	        -speedup performance laws
	        -scalability schemes and analysis
	        -scalable design principles

(4)	Multiprocessors, multicomputers and Massively Parallel Processing, MPP, systems
	        -interconnection networks
	        -MPP systems overview, programming concepts, current issues, key qualities
	         and examples.
	        -cache coherence protocols
	        -message-passing schemes
	        -shared-memory schemes
	        -memory organization in parallel processing systems

(5)	Advanced Topics
	        -introduction to pipeline/vector systems
	        -gigabit networks for parallel systems
	        -data flow paradigms
	        -Case studies

Course Regulations	
Exams	• The format for the exams is typically (but NOT always) as follows: General Definitions, Multiple-Choice, True/False, Analsis and Problem Solving, Short Essay Questions.
Makeup Exams	• Makeup exam should not be given unless there is a valid excuse.
Cheating	• Cheating or copying on exam or research project is an illegal and unethical activity. • Standard JU policy will be applied.

	• All graded assignments must be your own work (your own words).
Attendance	• Reasonable attendance is expected. • The University of Jordan policy requires the faculty member to assign ZERO grade (35) if a student misses 10% of the classes that are not excused. • Sign-in sheets will be circulated. • If you miss class, it is your responsibility to find out about any announcements or assignments you may have missed.